

Power LED indicator

Google LED 4 indicator

```

LP5024
IIC address setup
ADDR1 | ADDR0
-----
GND   | GND   -->010 1000 (Using)
GND   | VCC   -->010 1001
VCC   | GND   -->010 1010
VCC   | VCC   -->010 1011
Broadcast: 0X3C

LP5036
IIC address setup
ADDR1 | ADDR0
-----
GND   | GND   -->011 0000 LED pipe 1-12
GND   | VCC   -->011 0001 LED pipe 13-21, Status X1
VCC   | GND   -->011 0010 Others: Google 1-4,
VCC   | VCC   -->011 0011 Side LED L X2,
Broadcast: 0X1C Side LED R X2
                                  LED pipe 13-21, Status X1

```

LED Light Pipe

lu Cap is near closer to Connector.

Power and I2C from Main BOARD

VCC5.0V_2

VCC5.0V

502231-1500

S2

S1

S16

S15

S14

S13

S12

S11

S10

S9

S8

S7

S6

S5

S4

S3

S2

S1

LED2E_R

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

LED2E_G

LED2E_B

TP_L_R2

TP_L_R1

TP_L_G1

TP_L_G2

TP_L_R1

TP_L_B1

TP_GND1

GND3

1uF/50V/20mm

25.1

L side LED BOARD

1uF Cap is near Connector.

VCC5V_3

VCC5.0V

502231-1500

S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16 S17 S18 S19 S20 S21 S22 S23

LE027-R

LE027-G

LE028-R

LE028-G

LE029-R

TP_R_R2

TP_R_B2

TP_R_G1

TP_R_G2

TP_R_R1

TP_R_B1

TP_GND2

GND3

1uF

23.3

R side LED BOARD

[illegible]

SilkScreen: LED BOARD

NOTES:

1). If VDD33_DIG and VDD_I2S using +3.3V level, they can be powered by LDO33DIG_OUT

2). If CX20810 (pin27, pin45) powered by 3.3V, pin46 can short to pin45 to bypass the inner digital LDO

LDO33DIG_OUT:
Internal LDO 3.3V_D out,
can supply power for VDD33_DIG, VDD_I2S

VDD33_DIG:
Set Level for I2C, GPIO, MCLK
+3.3V or +1.8V

VDD33_I2S:
Set Level for I2S, RSTN
+3.3V or +1.8V

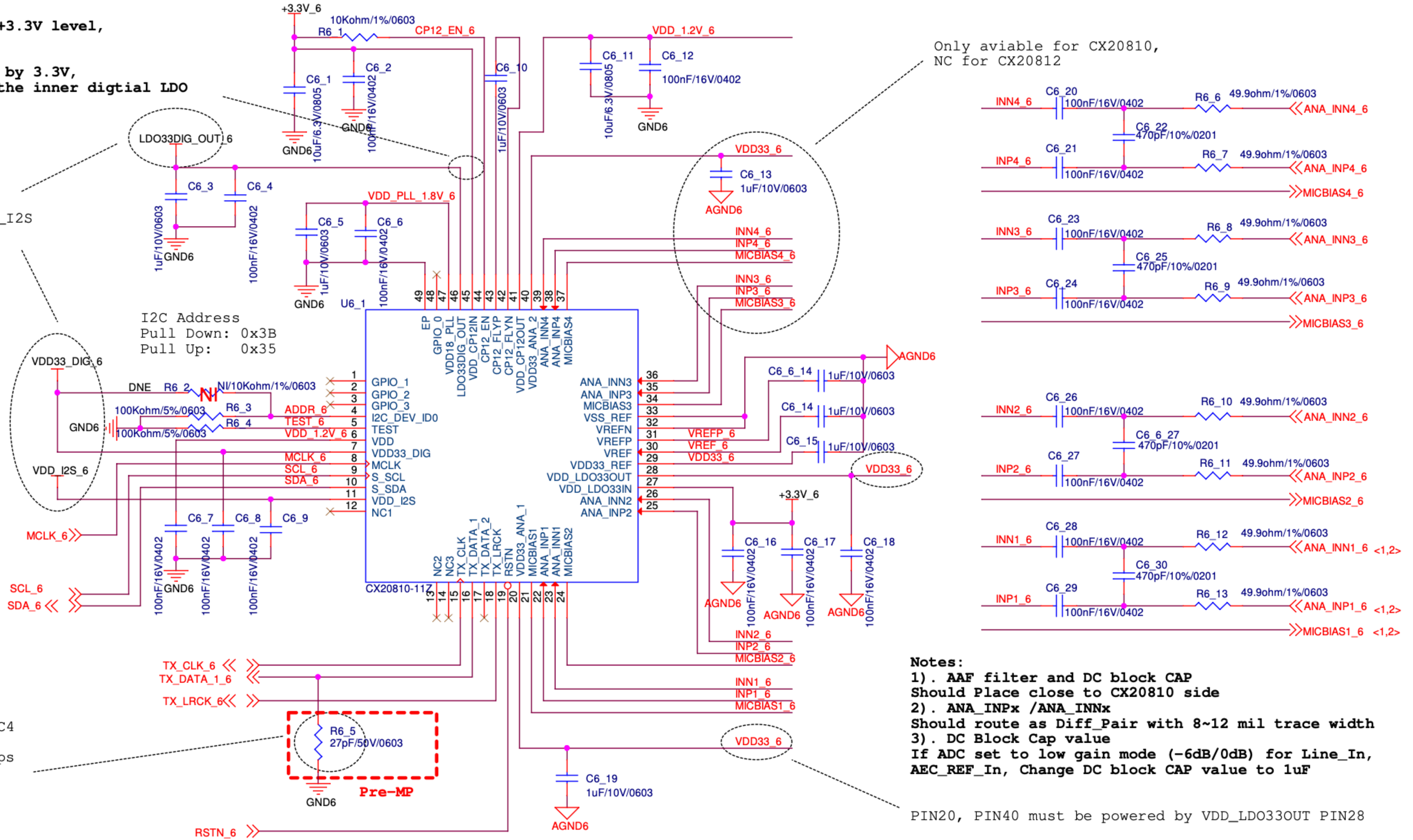
MCLK:
12.288MHz bypass PLL, or
900KHz to 50MHz with PLL active

I2C bus must pull up to
VDD33_DIG level at master site

I2S:
1). Normal Mode
TX_DATA_1 = ADC1 and ADC2
TX_DATA_2 = ADC3 and ADC4
2). TDM mode
TX_DATA_1 = ADC1, ADC2, ADC3 and ADC4
TX_DATA_2 = NA
3). TDM mode with multi CX20810 chips
Install pull down resistor R13

RSTN:(with internal pull up)
Must stay low for >=100 ms
after all power rails are stable.

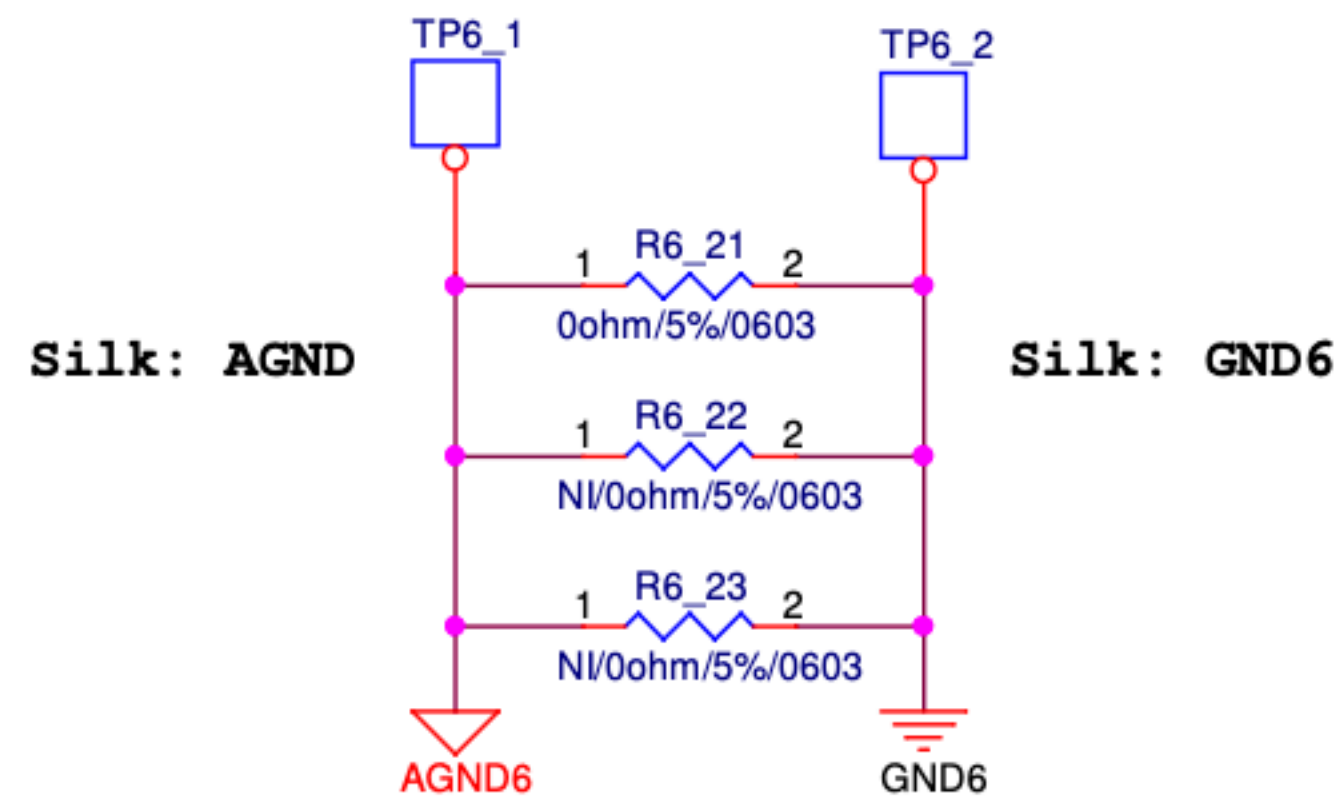
Only available for CX20810,
NC for CX20812



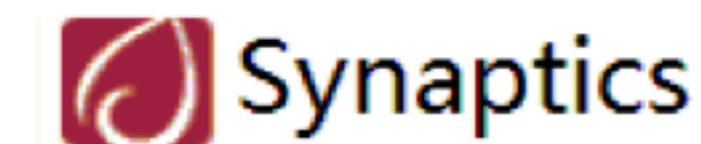
Notes:

- 1). AAF filter and DC block CAP
Should Place close to CX20810 side
- 2). ANA_INPx /ANA_INNx
Should route as Diff_Pair with 8~12 mil trace width
- 3). DC Block Cap value
If ADC set to low gain mode (-6dB/0dB) for Line_In,
AEC_REF_In, Change DC block CAP value to 1uF

PIN20, PIN40 must be powered by VDD_LDO33OUT PIN28



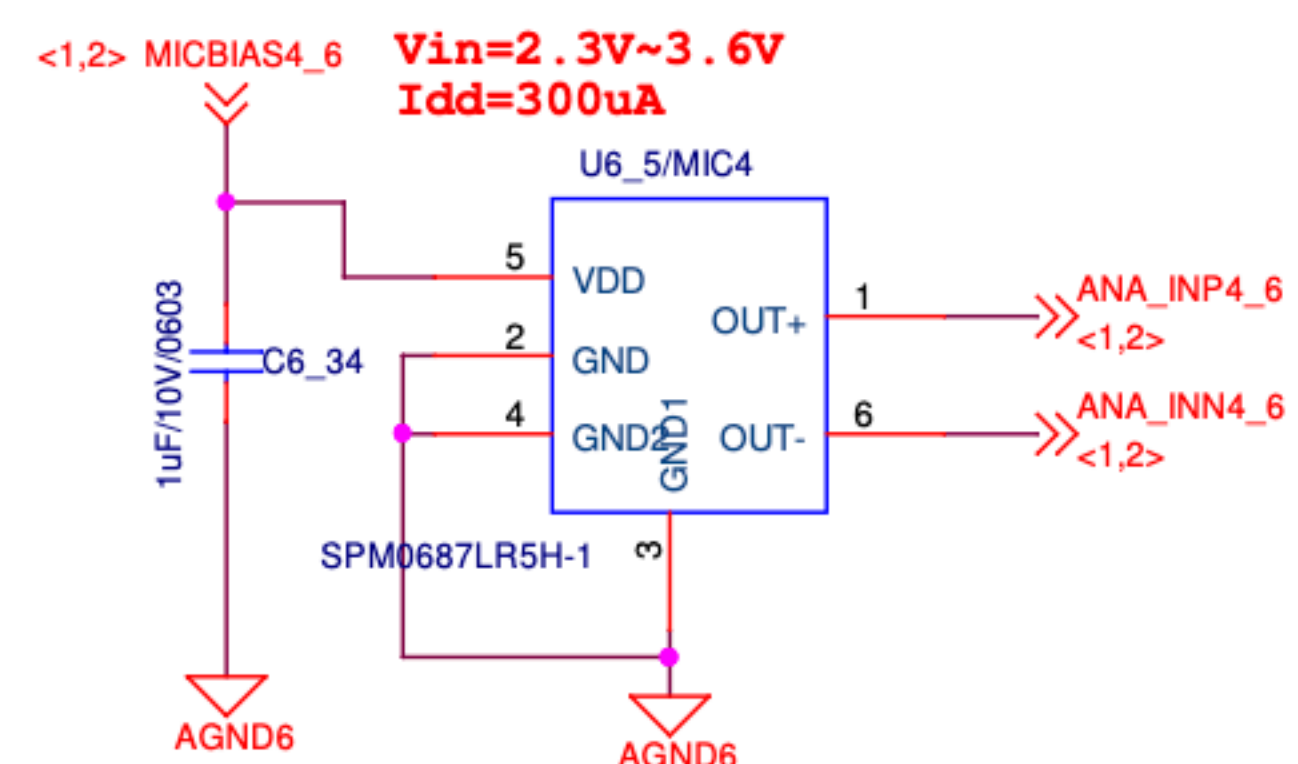
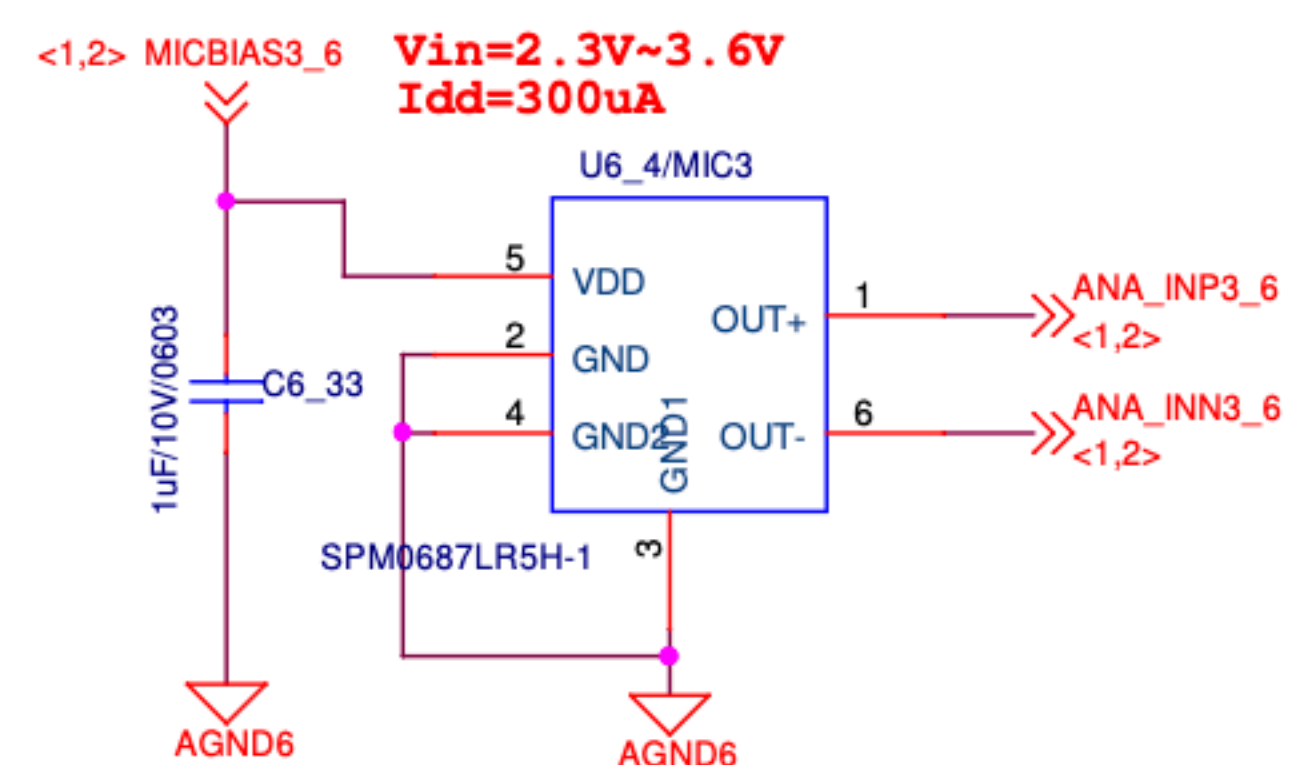
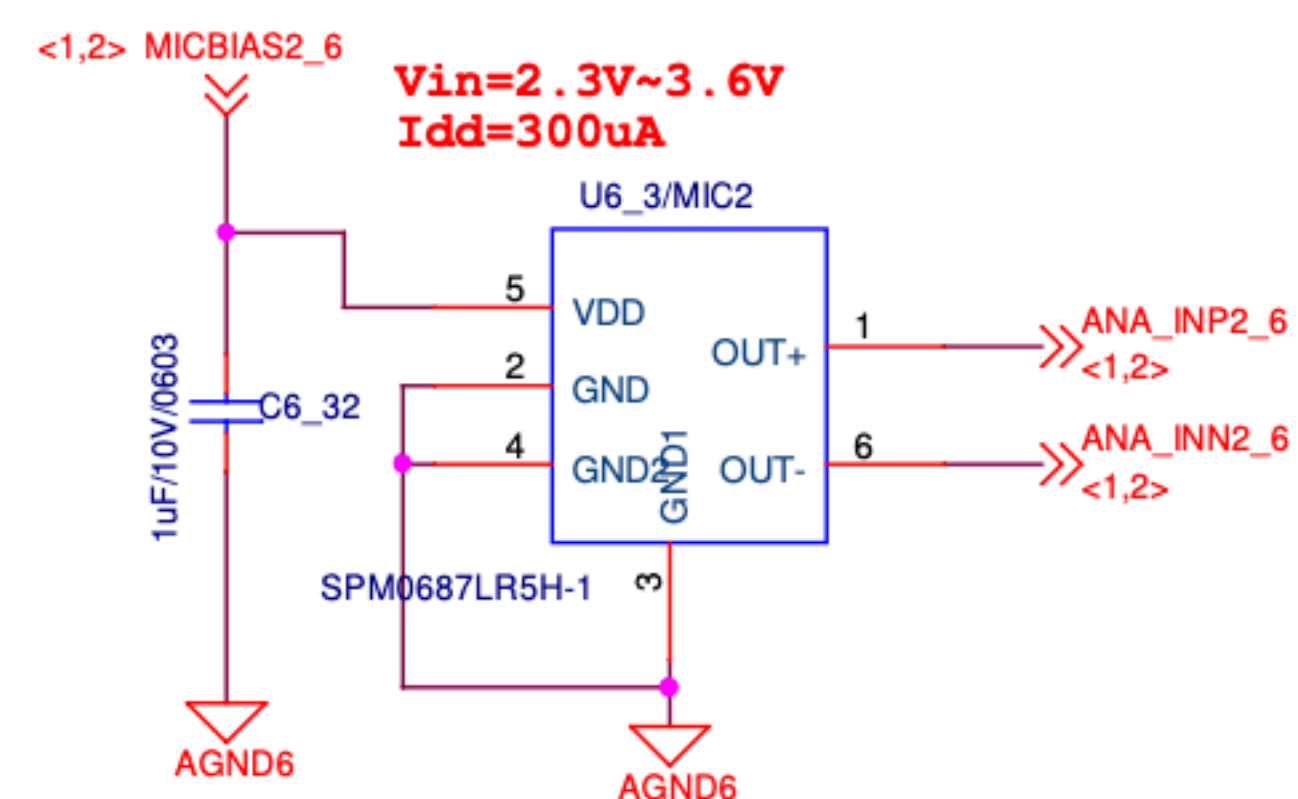
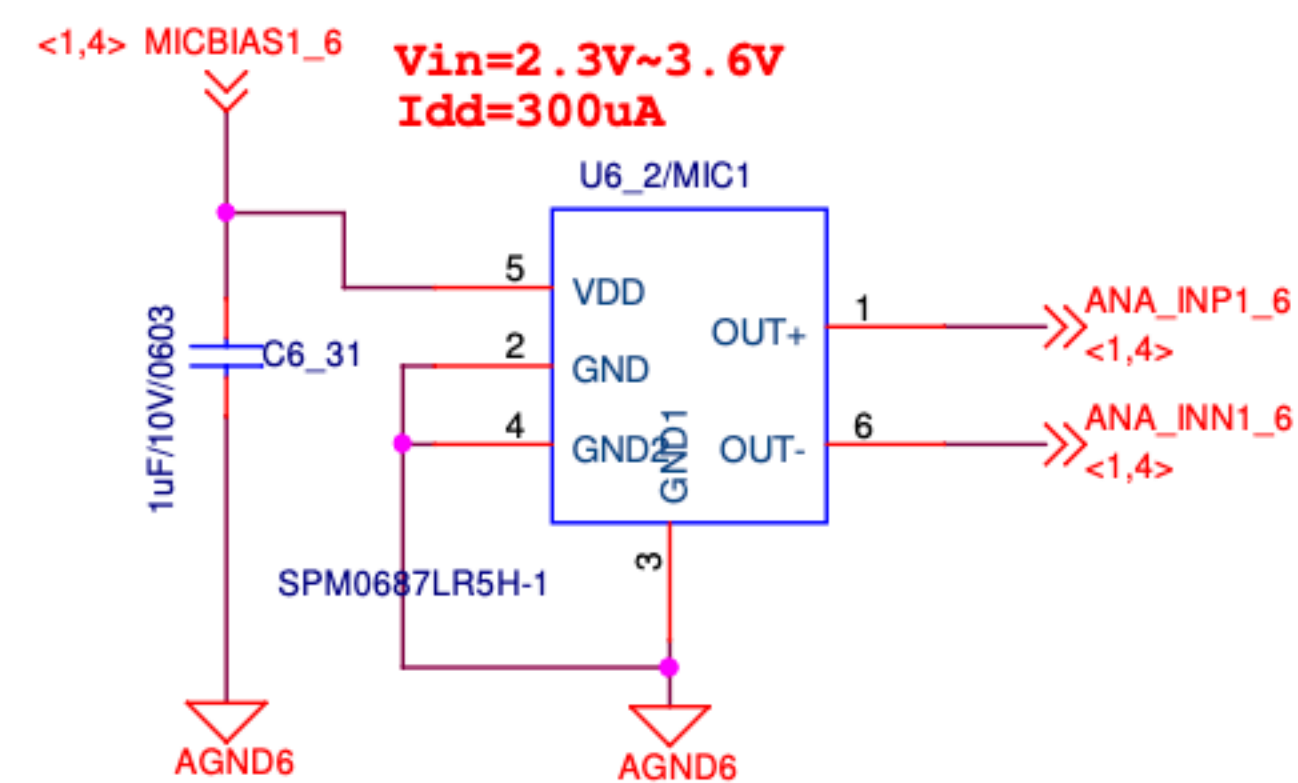
Short ANGD to GND directly with ~100mils wide trace



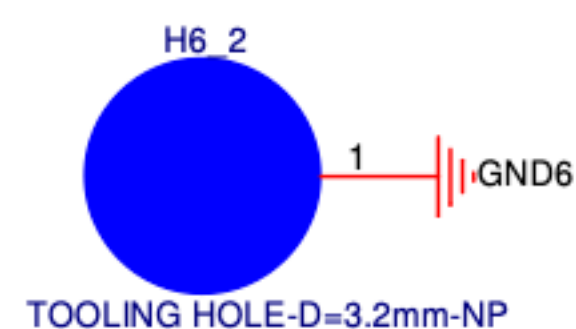
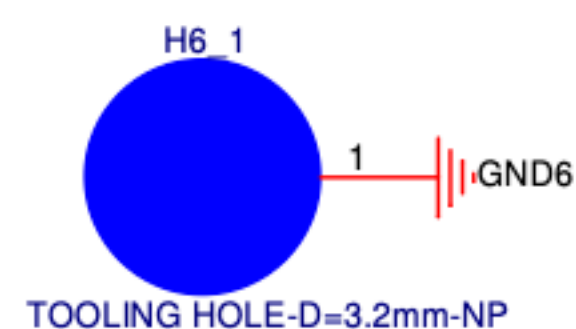
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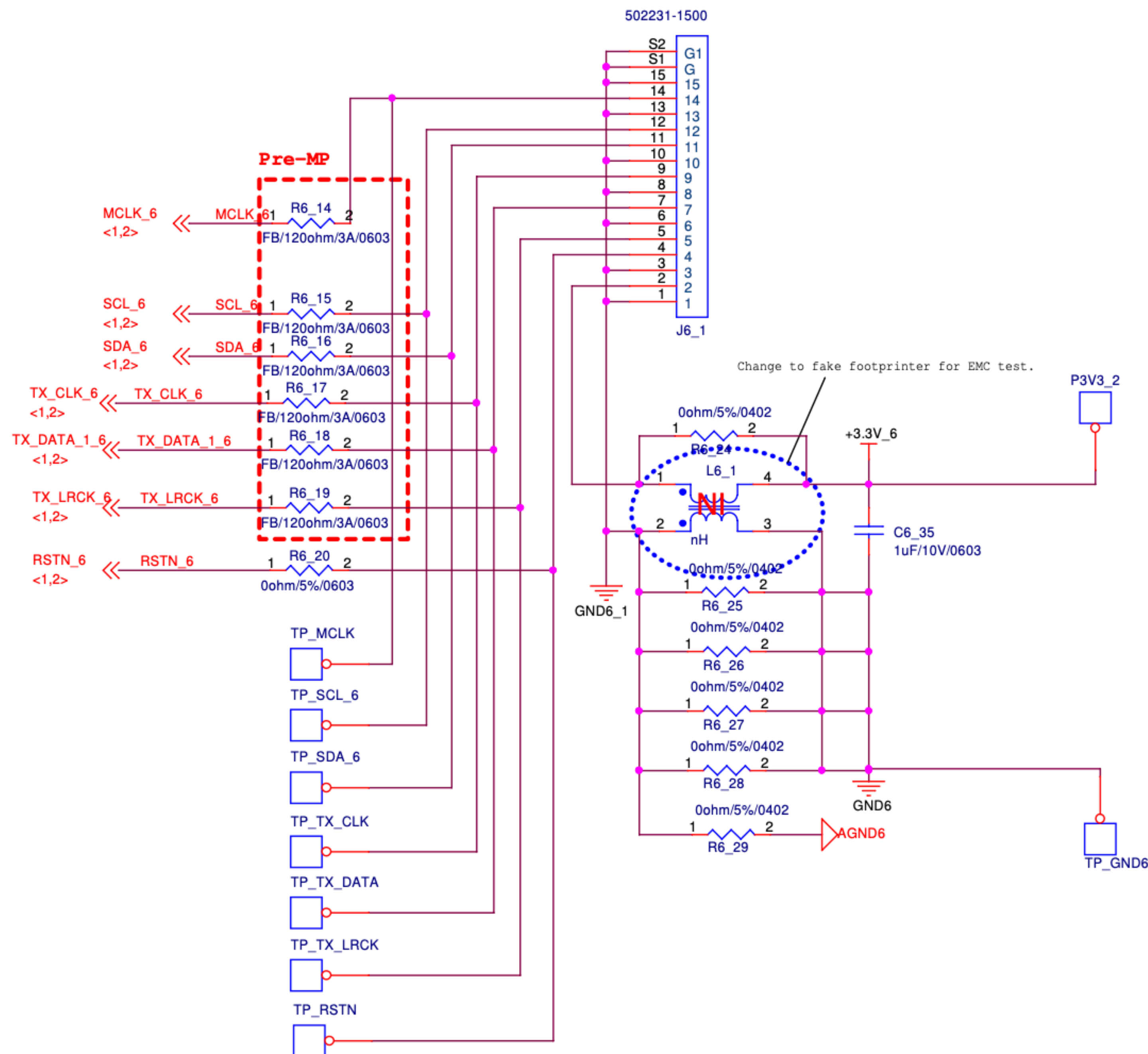
Title		K18X001T00-96.1516T00	
Sheet Title		MIC board-Straight	
Size B	Document Number	Rev 0.9	
Date	Monday, September 13, 2021	Sheet 1	of 2



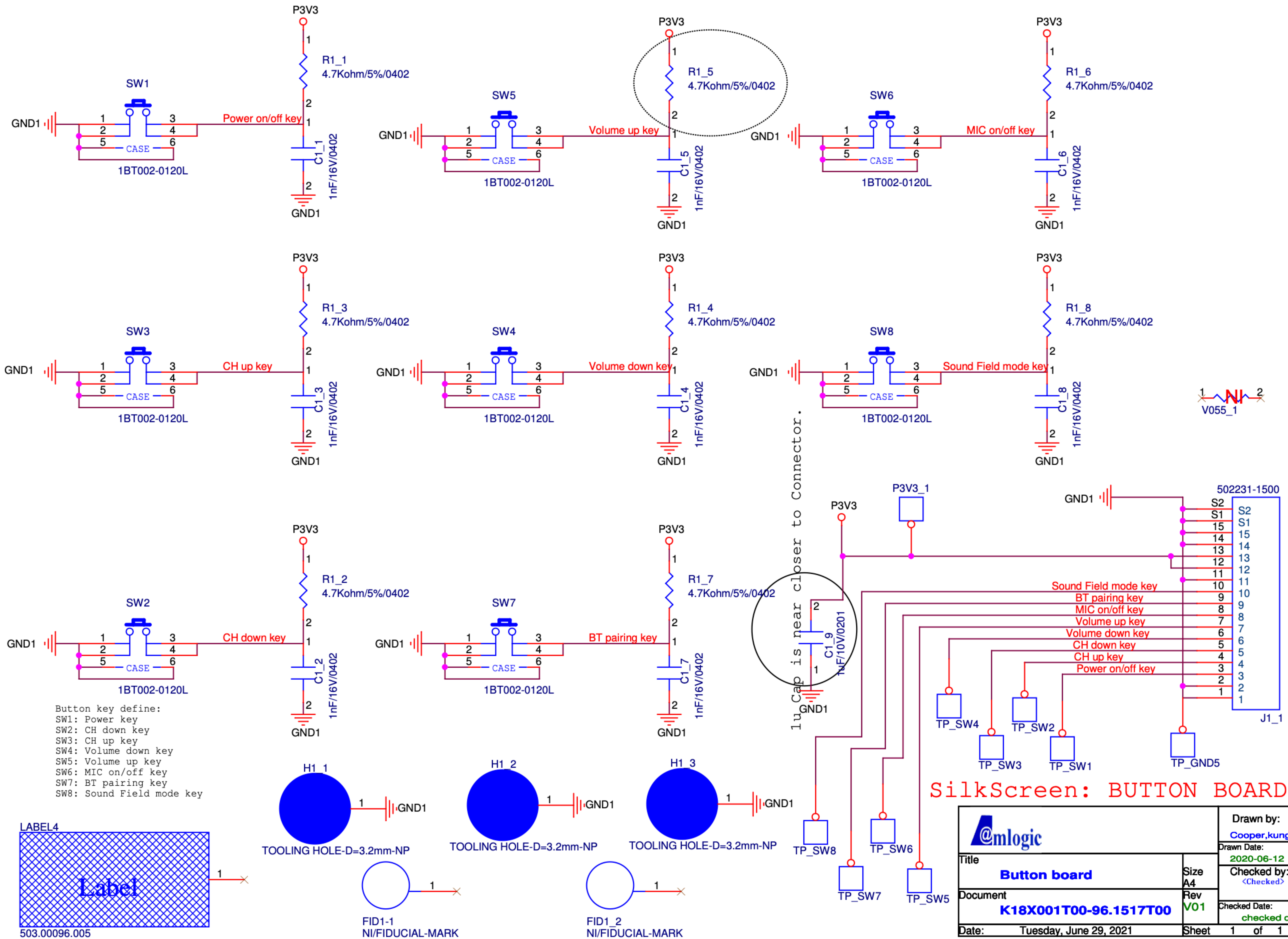
MIC placement define:
from left to right side
MIC1: U6_2
MIC2: U6_3
MIC3: U6_4
MIC4: U6_5



SilkScreen: MIC Curve BOARD



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Title K18X001T00-96.1516T00			
Sheet Title MIC board-Straight			
Size A3	Document Number		Rev 0.9
Date Monday, September 13, 2021	Sheet 2 of 2		



SilkScreen: BUTTON BOARD

@mlogic		Drawn by: Cooper,kung	
Title Button board		Drawn Date: 2020-06-12	
Document K18X001T00-96.1517T00		Checked by: <Checked>	
Date: Tuesday, June 29, 2021		Checked Date: checked date	
Sheet 1 of 1			

